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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 10/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,547	CHAUDHRY ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23-41* is/are allowed.

6)☒ Claim(s) *1-22 and 42-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/4/04 & 3/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's Pre-amendment filed 11/26/2003. Claims 1-45 were pending. Claims 46-66 were canceled.

Specification Objection

1. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the terms "offset spacers" as recited in claims 11 and 38 are not expressly mentioned in the specification.

Claim Rejections - 35 USC § 112

2. Claims 1-22,42-44 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

*** Re claim 1, line 15, "silicon plug" is lacking proper antecedent basis and indirect limitations.

*** Re claims 20,22, and 42,44: Independent claim 1 recites to form a vertical transistor having a gate in contact with the semiconductor plug, wherein the gate is of a second conductivity type. Claims 20, 22, and 42,44 recite "doped polycrystalline silicon",...,"metal" and "metal compound" such as of titanium, titanium nitride,..., aluminum, and copper. Although the gate of silicon is doped to a second conductivity type, metal and metal compound are not formed a gate of a second conductivity type for the JFET (note claims 21 and 43 in that silicon is not formed by electroplating).

(Dependent claims are rejected as depending on rejected base claim)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over. Hergenrother et al (6,027,975) taken with Choi et al (4,700,461) and Miyazawa (5,312,782).

Hergenrother et al. teach a method for forming a vertical transistor comprising at least the steps of: forming a first device region selected from the group consisting of a source region 205 and a drain region of a semiconductor device in a semiconductor substrate 200 (Fig 3A; col 8, lines 30-45); forming a multilayer stack comprising at least three layers 210/211/215/216/220 of material over the first device region in the semiconductor substrate wherein the second layer 215 is interposed between the first 210/211 and the third layers 216/220 and wherein the first layer 210/211 is proximate the first device region 205 (Fig 3B; col 8, line 46 through col 9); forming a window 225 in the at least three layers of material, wherein the window terminates at the first device region 205 formed in the semiconductor substrate 200; forming semiconductor material 230 of silicon, of a first conductivity type, within the window, thereby forming a semiconductor plug in the at least three layers of material, wherein the semiconductor plug has a first end, and a second end, and wherein the first end is in contact with the first device region 205 (Fig 3E; col 9, line 40 through col 10); forming a second device region selected from the group consisting of a source region and a drain region at the second end of the silicon plug 230, wherein one of the first and second device regions is a source region and the other is a drain region (Figs 3E, 3P; col 10, lines 4-13; col 11, lines 27-49); removing the second layer 215, thereby exposing a portion of the semiconductor plug 230 (Fig 3J; col 10, lines 45-53); and forming a gate 255/265 over a thin gate oxide 250 in contact with the semiconductor plug 230, wherein the gate 255/256 is doped

with one conductivity type (col 6, lines 18-29; col 9, line 64 through col 10, line 3). Claims 2-9 of this present application are respectively identical to claims 2,4-8,11-12 of Hergenrother (6,027,975). Claims 19-22 of this present application are respectively identical to claims 15,23-25 of Hergenrother (6,027,975). Re claim 10, wherein the layer of insulating material 211,16 comprises an etch stop layer 211,216 (col 8, line 63 through col 9, line 40). Re claim 11, wherein the layer of insulating material 211/216/240 comprises an offset spacer (Figs 3I-3K; col 10, lines 30-67). Re claim 12, the process further comprises the step of chemical mechanical polishing the surface of the substrate after forming the semiconductor plug 230, wherein the chemical mechanical polishing planarizes the semiconductor plug with the third layer of the multilayer stack (col 11, lines 50-57). Re claim 13, wherein the top layer 220 of material in the multilayer stack comprises a stop for chemical mechanical polishing (col 11, lines 50-57). Re claim 14, wherein the top layer as the third layer 220 comprises a silicon nitride (col 12, lines 48-52). Re claim 17, wherein the gate as region of one conductivity type is surrounding the semiconductor plug 230 of a first conductivity type (Fig 3N, col 11, lines 23-26; col 6, lines 17-29; col 8, lines 26-30).

Hergenrother et al teach forming a MOSFET with a thin gate oxide 250 formed between the gate 255/256 and the semiconductor plug 230; whereas, claim 1 recites a gate 255/256 in contact with the semiconductor plug 230 (i.e. for forming a JFET), wherein the gate is of a second conductivity type, and wherein, re further claim 18, and the gate is doping a region the plug to form a pn junction.

However, Choi et al teach (at col 1, lines 10-67; Fig 1; cols 4-5) about forming a MOSFET and JFET, wherein the MOSFET is generally different from the JFET in that "a gate is formed above the channel, but is insulated from the semiconductor material by a thin oxide layer (usually SiO_2)..." (col 1, line 30-55), wherein, as shown in Figure 1, steps V and VI, the JFET comprises a gate 30 of a second conductivity type in contact with a semiconductor plug channel, wherein dopant impurities of the second conductivity type is diffused to dope the semiconductor channel plug 24 from the gate 30 to form a pn-junction 32 (col 4, line 51 through col 5). Miyazawa also teaches about forming a vertical MOSFET (Fig 10G; cols 11-12) and a vertical JFET (Fig 11; col 12, lines 12-21), wherein "the vertical channel includes no gate

insulating film" (col 12, lines 12-21), and wherein the gate electrode 119 has a reverse second conductivity type of the semiconductor plug 111 of a first conductivity type.

Therefore, the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the method for forming a MOSFET of Hergenrother '975 by forming a JFET including no thin gate oxide between the gate and the semiconductor plug, so that the gate is in contact with the semiconductor plug and forms a pn junctions by doping the semiconductor plug from the gate, as taught by Choi and Miyazawa. This is because of the desirability to form another different type of semiconductor device, namely, a junction field effect transistor (JFET), wherein the JFET is more suitable for high temperature operation since there is no gate oxide, and wherein the JFET is also less sensitive to total dose radiation.

5. Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hergenrother et al (6,027,975) taken with Choi et al (4,700,461) and Miyazawa (5,312,782), as applied to claims 1-22, and further of Fitch et al (5,414,289).

The combined references including Hergenrother, Choi, and Miyazawa teach a method for forming a junction field effect transistor as applied to claims 1-22 above.

The references including Hergenrother teaches forming a junction field effect transistor; whereas, a Claim 45 recites forming a matched junction field effect transistors by duplicate forming at least two first and second windows in the multilayer stack, forming two first and second semiconductor plugs, and two doped regions (gates) for surrounding the two semiconductor plugs.

However, Choi teaches (at col 5, lines 65 through col 6, lines 45; Figs 3 and 1) forming a plurality of junction field effect transistors at the same time by forming a least two doped region gates 30 over the two semiconductor plug layer formed between two first and second windows formed between the LOCOS oxide regions 26. Fitch teaches forming a plurality of field effect transistors by at least forming two first and second windows (Figs 5-6,7; col 6, lines 17-22, lines 35-51; Figs 9,11, line 64 through col 7) in the multilayer stack, forming two first and second semiconductor plugs (Fig 9, 48/50/52/54 and 56/58/60/62), and two doped region gates 18 for surrounding the two semiconductor plugs 48/50/52/54.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a plurality of matched junction field effect transistors of the combined references including Hergenrother, Choi, and Miyazawa by forming at the same time at least two first and second windows in the multilayer stack, two first and second semiconductor plugs, two doped region gates for surrounding the two semiconductor plugs, as taught by Choi and Fitch. This is because of the desirability to form a plurality of matched junction field effect transistors at the same time so as to reduce production cost and time.

Allowable Subject Matter

6. Claims 23-41 are allowed.

7. The following is an examiner's statement of reasons for allowance

The references including Hergenrother (6,027,975), Choi et al (4,700,461), Miyazawa (5,312,782), Fitch et al (5,414,289), etc., of record, alone or in combination, do not anticipatively disclose each and every aspect of the claimed method, or fairly make a prima facie obvious case of the claimed method, in combination with other processing claimed limitations as recited in base claim 23, the inclusion of forming a first and a second semiconductor plug within the first and second windows formed in the at least three layers of material, wherein each of the semiconductor plugs has a first and second ends, and wherein the first end of each semiconductor plug is in contact with the first device region, and wherein the first semiconductor plug is of a first conductivity type; forming a second device region selected from the group consisting of a source region and a drain region at the second end of the first semiconductor plug, wherein one of the first and second device regions is a source region and the other is a drain region; forming a third device region selected from the group consisting of a source region and a drain region at the second end of the second semiconductor plug, wherein one of the first and the third device regions is a source region and the other is a drain region; removing the second layer, thereby exposing a portion of the first and the second semiconductor plugs; forming a layer of dielectric material on the exposed portion of the first semiconductor plug; forming a region of a second conductivity type surrounding the first conductivity type region of the second semiconductor plug; and forming a gate having a first region in contact with the layer of dielectric material and

having a second region in contact with the second conductivity type region of the second semiconductor plug.

****

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-01

Michael Trinh
Primary Examiner